

SEMICONDUCTOR INTEGRATED CIRCUITS LAYOUT-DESIGN (AMENDMENT) RULES, 2012

gao•-33004/99 REGD. NO, 1). L.-33004/99 Che Gazette of •tidia Nu 4561 EXTRAORDINARY PART 11—Section 3—Sub-section (i) PUBLISHED BY AUTHORITY 14, 2012AR 23, 1934 NEW DELHI, FRIDAY, SEPTEMBER 14, 20'2/BHADRA 23, 1934 , 14 , 2012 -qfi--qu e.fifi4H, 2000 (2000 37) 96 (2) g•q, . 2001 2012 2001 (3) KPE" *TIE" "aaa 1)f201 Zi. 3479 Glf2012 MINISTRY OF COMMUNICATIONS AND INFORMATION TECHNOIDGY (Department of Electronics and Information Technology) NOTIFICATION New Delhi, the 14th September, 2012 GS.R. 689(E).—In exercise of the powers conferred by the sub-section (2) of Section 96 of the Semiconductor Integrated Circuits Layout-Design Act, 2000 (37 of 2000), the Centrat Govemment here by makes the following rules to amend the Semiconductor tntegrated Circuits Layout-Design Rules, 2001 namely : 1. (l) These rules may be called the Semiconductor Integrated Circuits Layout-Design (Amendment) Rules, 2012 (2) They shall come into force on lthe date oftheir publication. 2.In the Semiconductor Integrated Circuits Layout-Design Rules, 2001 in rule IO, (b) Printed by the Manager. Government of India Press. Ring Road. and Published by the Controller of Publications. in sub-rule (3), the words "by the bank draft", the words "by a bank draft payable to the Pay & Accounts Officer, Department of Electronics and Information Techno'ogy" shan be substituted; in sub-rule (4), for the words • •made payable to Registrar", *he words "made payable to the Pay & Accounts Officer, Department of Electronics and Information shall be substituted. [F. No. I Y201] -SICLDR] Dr. ANITA BHATNAGAR JAIN, Jt. secy. Mayapuri. New Delhi-1 10064 Delhi-1 10054